This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

Claims 1-13 - deleted

19. (As Filed) A method of fabricating an integrated circuit, the method comprising:

providing a plurality of inverters as part of said integrated circuit;

providing a plurality of MACROs as part of said integrated circuit;

providing a second layer of metallization;

utilizing no local interconnect in said second layer of metallization to configure said plurality of inverters;

utilizing said second layer of metallization to connect at least two of said MACROs.

20. (As Filed) The method as described in claim 19 and further comprising:

utilizing in at least one of said MACROs no local interconnect within said second layer of metallization.

21. (As Filed) The method as described in claim 19 and further comprising:

utilizing in a plurality of said MACROs no local interconnect within said second layer of metallization.

22. (As Filed) The method as described in claim 19 and further comprising:

utilizing in all of said MACROs no local interconnect within said second layer of metallization.

23. (As Filed) The method as described in claim 19 and further comprising;

embedded at least one of said MACROs within a standard cell array of said integrated circuit.

24. (As Filed) The method as described in claim 23 wherein said standard cell array comprises a row pitch, said method further comprising:

utilizing a MACRO having a row pitch equivalent to said standard cell array.

30. (As Filed) An integrated circuit, comprising:

a logic inverter comprising:

an n-channel field effect transistor;

a p-channel field effect transistor;

a gate, formed in a layer of polysilicon; and

a drain of the p-channel field effect transistor and a drain of the n-channel field effect transistor formed in said same layer of polysilicon.

31. (As Filed) The integrated circuit as described in claim 30, wherein the polysilicon comprising said gate is coplanar with the polysilicon comprising said drain of the p-channel field effect transistor and said drain of the n-channel field effect transistor.

32. (As Filed) The integrated circuit as described in claim 30, further comprising:

a second layer of metallization, wherein the second layer of metallization comprises substantially no local interconnect.

33. (As Filed) The integrated circuit as described in claim 32, wherein said second layer of metallization comprises no local interconnect.

34. (As Filed) The integrated circuit as described in claim 30, further comprising:

a plurality of MACROs; and

a second layer of metallization interconnecting said plurality of MACROs.

35. (As Filed) The integrated circuit as described in claim 30, further comprising:

a trace, formed in said layer of polysilicon, wherein said trace connects said drain of said p-channel field effect transistor and said drain of said n-channel field effect transistor.

36. (As Filed) The integrated circuit as described in claim 35, further comprising, no local interconnect within said second layer of metallization in at least one of said MACROs.

37. (As Filed) The integrated circuit as described in claim 35, further comprising, no local interconnect within said second layer of metallization in a plurality of said MACROs.

38. (As Filed) The integrated circuit as described in claim 35, further comprising, no local interconnect within said second layer of metallization in all of said plurality of MACROs.

39. (As Filed) The integrated circuit as described in claim 35, wherein at least one of said MACROs is comprised by a standard cell array of the integrated circuit.

40. (As Filed) The integrated circuit as described in claim 39, wherein said standard cell array comprises a row pitch and at least one MACRO has a row pitch equivalent to the row pitch of said standard cell array.